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CARRIER OBJECTIVES

Motivated and research-driven candidate in Electronics and Communication Engineering, with a specialization in VLSI Design, seeking a challenging **Assistant Professor** position to contribute to cutting-edge research and development in semiconductor technologies, low-power design, and advanced digital/ analog systems. Eager to collaborate with interdisciplinary teams, publish impactful research, and further advance the frontiers of integrated circuit design through innovation, critical thinking, and academic excellence.

EDUCATIONAL QUALIFICATIONS

Qualifications	University
Ph.D	NIT Hamirpur
Masters (VLSI Design)	NIT Kurukshetra
Graduation / Under graduation	VTU, IIT Madras

ACHIEVEMENTS

- Qualified **GATE** Exam.
- Qualified **UGC NET**.
- Secured **all India rank one** in M. Tech entrance exam in GBU.
- Qualified **IIT Madras** entrance examination for degree level.

KNOWLEDGE OF TOOLS AND LANGUAGES

- Worked on **Cadence** and **Xilinx** tool.
- Worked on **TCAD** Tools like **SILVACO Atlas, and Synopsys**.
- **C, C++, Verilog,** sand **MATLAB**.
- **Operating System:** Fedora flavour of **LINUX,** WINDOWS.

EMPLOYERS (WORK EXPERIENCE)

- **Graduate Engineer Trainee** in **Sterlite Technology**, Ahmedabad.
- **Analog Design Engineer** in **TBRL-DRDO**, (Atech India Pvt. Ltd.), Chandigarh.
- **TSA** in **Lenovo India Private Limited**, Bangalore.

ACADEMIC PROJECTS

Project 1- Analog Design of 3-D FinFET using Synopsys TCAD

DESCRIPTION: FinFET, Fin Field Effect Transistor, is a type of non-planar or "3D" transistor used in the design of modern processors. I worked on designing of FinFET at device level and extracted the analog performance like transconductance(g_m), output conductance (g_{ds}), Voltage gain (A_v), gate Capacitance (C_{gg}), and unity gain cut-off frequency(f_T). FinFET have improved current driving capability, then MOSFET. It shows better short channel control.

Project 2-Analog performance of Junctionless transistor using Silvaco TCAD

DESCRIPTION: Some of the process challenges for scaling the CMOS devices can be reduced by devices which do not need any junctions and this is the main advantage of junctionless transistor unlike the conventional MOSFET, JLTs have heavy channel doping and is fully depleted in the OFF state. I worked on analog/RF performance of dual-k spacer (Dual-kS) trigate junctionless transistor (JLT) and investigated with respect to the parametric variations. The Dual- kS JLT improves analog/RF figure of merits (FOMs) and shows its lower dependence to the parametric variations compared with the conventional (low-k spacer) JLT. This study reveals that the design of Dual-kS JLT with lower aspect ratio (1 to 3) improves the analog FOMs with moderate frequency of operations at fin height and thickness of 10 nm with gate length being 15nm. frequency of operation can be increased further by increasing the aspect ratio (4 to 6) without sacrificing the analog FoMs such as transconductance(g_m), output conductance (g_{ds}), Voltage gain (A_v).

Project 3 – Radiation hardened using Cadence Virtuso

DESCRIPTION: Radiation can affect electronic devices both in transistors and at the IC level, mainly focusing on CMOS SRAMs. This project also provides ways to address these problems such as small design changes and sophisticated fabrication methods. At this level, radiation introduces a number of important issues. Because charges collect in the oxide and interfaces, the threshold voltage moves which can cause transistors to behave malfunction. Standby power, increased leakage and radiation-triggered leakage paths are what cause subthreshold slope degradation.Decreased transconductance is caused by a loss of mobility from impacts of charge scattering which makes analog circuits less able to amplify signals.

Project 4 – Smart Vision Testing using ATMEGA328P Arduino

Project 5 – Smart RTC Callender using Arduino

List of International Journals

1. **Sachindra Bharti**, Rohit Dhiman and Gargi Khanna, "Performance Investigations of Novel Hybrid Junctionless Double Gate Transistor with Gate Engineering," ***Journal of Active and Passive Electronic Devices Journal,*** vol.17(4), pp.329-345, December 2023**.**
2. **Sachindra Bharti**, Rohit Dhiman and Gargi Khanna, "Temperature Performance Analysis of Hybrid Junctionless Double Gate Transistor," ***Journal of Active and Passive Electronic Devices Journal Journal,*** vol.18, (1) pp.19, January 2024.
3. **Sachindra Bharti**, and Gargi Khanna, "Assessment of Pocket Inside Junctionless Hybrid Double Gate Transistor for Low Power Circuit Applications," ***ECS Journal of Solid-State Science and Technology,*** vol.15, (2) pp.19, February 2026.
4. **Sachindra Bharti**, Rohit Dhiman and Gargi Khanna, "Engineering Oxide Stacks in Junctionless Double Gate Transistors," I***nternational Journal of Numerical Modelling: Electronic Networks, Devices and Fields. (under review).***
5. **Sachindra Bharti**, Rohit Dhiman and Gargi Khanna, "Analog Performance of Novel Hybrid Junctionless Double Gate Transistor with Gate Engineering", ***Microelectronics Journal***. **(Communicated).**

List of International Conference

1. **Sachindra Bharti**, Rohit Dhiman and Gargi Khanna, "Body Bias of Junctionless Transistors for Analog Applications", 4th International Conferences in Nanoelectronics, Machine Learning, Internet of Things and Computing Systems (NMIC-2024), Jharkhand, India, April 2024, pp. 1-6. (**Best Paper Award**).
2. **Sachindra Bharti**, and Gaurav Saini, "Sensitivity Analysis of Junctionless FinFET for Analog Applications", 2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS), Madurai, India, 2018, pp. 1288-1293, doi: 10.1109/ICCONS.2018.8662918.

SUBJECT TAUGHT / WILLING TO TEACH

1. Electronic Devices	**2. Digital Electronics**	**3. Analog Circuits**
4. Electromagnetic Theory	**5. Basic Electrical circuits**	**6. Basic Electronics**

Trainings / Workshop Undertaken

Sl. No.	Name of the Organizing Institute	Title	Dates
01	**NIT Hamirpur**	**Electrical Design of Advanced VLSI and Communication Systems**	26-02-2024
02	**NIT Delhi**	**IEEE International** Workshop **on Silicon Photonics**	05-02-2024
03	**NIT Andhra Pradesh**	**"Challenges & Innovation in Antennas for Wireless Connectivity"**	05-02-2024
04	**NIT Jalandhar**	**Current Trends in Submicron Device and Circuit Design**	26-06-2023
05	**DAIICT Gujrat**	**High End Workshop on Hardware-Assisted Security for Fog Computing-based IoT Network**	26-06-2023
06	**AMD- Xilinx**	**Designing with Versal Adaptive SoC: Architecture and Methodology**	04-09-2023
07	**NIT Hamirpur**	**Nanoscale Device**	01-07-2021
08	**MATHWORKS & NIT Kurukshetra**	**MATLAB & SIMULINK**	30-07-2018
09	**IIT DELHI, Tryst-2018**	**IOT with ARDUINO**	26-02-2018
10	**IIT DELHI, Tryst-2018**	**C++**	25-02-2018
11	**IIT DELHI, Tryst-2018**	**8051 Embedded system**	24-02-2018
12	**NIT Kurukshetra**	**International conference**	20-01-2018

13	**IIITDM JABALPUR**	**Nano Electronics devices**	26-06-2017
14	**NIT Kurukshetra**	**IOT**	2017
15	**IIT MADRAS**	**Electrical Circuits**	2012

References

Dr. Gargi Khanna, Associate Professor	DoECE, NIT Hamirpur, HP, India
Dr. Rajeevan Chandel, Professor	DoECE, NIT Hamirpur, HP, India
Dr. R.K. Sharma, Professor	DoECE, NIT Kurukshetra, HP, India

EXTRA CURRICULAR ACTIVITY

- Participated in IIT Delhi Technical fest.
- Regular participation in society programs.
- Organized classes in summer/winter for financially challenged student.
- Joined NCC and achieved grade "A".
- Joined Bharat Scout and Guide.
- Teaching Economically Challenged students in free time.

KEY RESPONSIBILITIES HANDLED

- Worked as an Analog Design Engineer.
- Presenting the Design in front of superiors.
- Implementing the suggestions in the plan/ Design.
- design reviews across the organization.
- Ensuring that work should be done on time.
- Excellent at assessing the resources and identifying the opportunities.
- Excellent in coordinating with co-workers.

HOBBIES

- Movies, Cooking, Traveling, Music.

DECLARATION

I hereby declare that above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

Date: 07-04-2026 Place: IIIT Bhagalpur Signature