Dheeraj Kumar Sinha

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AREAS OF INTEREST: I/O Devices & Circuits,ESD Protection Circuits,Device-Circuit Interaction,Semiconductor Device Modelling.

ACADEMIC QUALIFICATIONS:

Degree	Year	Institution	CGPA/Percentage
Ph.D Electronics & Electrical Engineering VLSI (Microelectronics)	2012-2017	Indian Institute of Technology Guwahati	7.73/10
B.Tech Electronics and Communication Engineering	2006-2010	Rajiv Gandhi Technical University, Bhopal Madhya Pradesh	75.19/100

PROFESSIONALBACKGROUND:

Designation	Year	Organisation
Assistant Professor	July 2017 – till present	Indian Institute of Information Technology Bhagalpur
Research Associate	Feb 2017 – June 2017	Indian Institute of Technology Guwahati

SELECTED PUBLICATIONS

1. **Dheeraj Kumar Sinha,** M. S. Ansari, Ashok Ray, Gaurav Trivedi, Amitabh Chatterjee and Ronald D. Schrimpf, "*Fast Ionization-front Induced Anomalous Switching Behavior in Trigger Bipolar Transistors of Marx-bank Circuits Under Base-drive Conditions"* IEEE Transactions on Plasma Science, Vol. 46, no. 6, pp. 2064-2071, June 2018.
2. **Dheeraj Kumar Sinha,** and Amitabh Chatterjee, *"Spice Level Implementation of Physics of Filamentation in ESD Protection Devices"* Microelectronics Reliability (Elsevier), Vol. 99, pp. 239-247, Dec 2017.
3. Saurav Roy, Amitabh Chatterjee, **Dheeraj Kumar Sinha,** Rimma Pirogova and Srimanta Baishya, *"2-D Analytical Modelling of Surface Potential and Threshold Voltage for Vertical Super-Thin Body Field Effect Transistor"* IEEE Transactions on Electron Devices, Vol. 64, pp. 2106-2112, Apr 2017.
4. **Dheeraj Kumar Sinha,** Amitabh Chatterjee and Gaurav Trivedi, *"Two Dimensional Numerical Simulator for Modeling NDC Region in SNDC Devices",* Journal of Physics: Conference Series, vol. 759(1), pp. 012099, Sept-2016**.**
5. **Dheeraj Kumar Sinha,** Amitabh Chatterjee and Ronald D. Schrimpf, "*Modeling Erratic Behavior Due to High Current Filamentation in Bipolar Structures Under Dynamic Avalanche Conditions*" IEEE Transactions on Electron Devices, Vol. 63, no. 8, pp. 3185-3192, Aug 2016.
6. **Dheeraj Kumar Sinha,** Vishnuram Abhinav, Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, "*A Novel Capacitorless DRAM Cell Design Using Band-Gap Engineered Junctionless Double-Gate FET*", 29th IEEE International Conference on VLSI Design, Kolkata, Jan. 2016.
7. Vishnuram Abhinav, **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Forrest Brewer, "*A Novel Co-design Methodology for Optimizing ESD Protection Device Using Layout Level Approach*", 29th IEEE International Conference on VLSI Design, Kolkata, Jan. 2016.
8. **Dheeraj Kumar Sinha,** Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, *"Design of Band-gap Engineered Silicon-Germanium Junctionless Double-gate FET for ZRAM application*", 6th International Conference on Computers and Devices for Communication, Kolkata, Dec. 2015.
9. **Dheeraj Kumar Sinha,** Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, *"Analysis and Design of ZRAM Cell for Low Voltage Operations",* 18th International Workshop on Physics of Semiconductor Devices, Bangalore, Dec. 2015.
10. Vishnuram Abhinav, **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Rajan Singh**,** *"Methodology for optimizing ESD protection for high speed LVDS based I/Os*", 19th International Symposium on VLSI Design and Test, Ahmedabad, June, 2015.
11. Ashok Ray, Gaurav Kumar, Sushanta Bordoloi, **Dheeraj Kumar Sinha**, Pratima Agarwal and Gaurav Trivedi, "F*EM based Device Simulator for High Voltage Devices*", 21st International Symposium on VLSI Design and Test (VDAT), Roorkee, Apr-2017.
12. Saurav Roy, Shiva Puri Goswami , **Dheeraj Kumar Sinha,** Amitabh Chatterjee, and Victor Koldyaev, *"Use of RTA in Super-thin Body Structures to Replace Critical Implants",*18th International Workshop on Physics of Semiconductor Devices, Bangalore, Dec. 2015.

TEACHING EXPERIENCE:

1. **Courses Taken:**
   - Basic Electronic Circuits (3-0-0-3)
   - Digital Design (3-0-0-3)
   - Semiconductor Devices (3-1-0-4)
   - VLSI Design (3-0-0-3)

2. **LAB Courses Taken:**
   - Basic Electronics Lab (0-0-3-3)
   - Digital Design Lab (0-0-3-3)
   - VLSI Design Lab (0-0-3-3)

LABORATRY DEVELOPED AND SETUP AT IIITBH:

1. Analog & Digital Electronics Laboratory (UG)
2. Communication Laboratory (UG)
3. VLSI & DSP Laboratory (UG)
4. Microwave & Design Laboratory

ADMINISTRATIVE POSITION AND ADDITIONAL RESPONSIBILITIES:

1. Head of the Department, Electronics & Communication Engineering (Since May-2019)
2. Faculty Incharge, Civil Works (Since May-2019)
3. Faculty Incharge, Media & Spokesperson (Since July-2019)
4. Coordinator, Student Affairs (Since Oct-2018)
5. Faculty Advisor, ECE Branch (Since July-2017)
6. Warden, Boy's Hostel, IIIT Bhagalpur (Since July-2017 to Sept-2018)
7. Chairman, Anti-ragging committee (Since July-2017)
8. Convenor, Food Committee Inspection team
9. IIIT Bhagalpur, UG Admission in-charge-2017

TECHNICAL SKILLS:

1. **Operating System:** Linux, MS windows.
2. **Tools:** TCAD Sentaurus, MATLAB, Mentor Graphics, Cadence Spectre, Cadence Virtuoso, HSPICE, NGSPICE, Latex.
3. **Hardware:** DSO, Function Generators, B1500A Semiconductor Device Analyser.

OTHER TECHNICAL EXPERIENCE:

1. Designed optimized Protection circuits without affecting the ESD robustness (Layout optimization) in 0.18μm bulk technology.
2. The impact of ESD parasitics on the CIS/CCD Image sensor performance was analysed based on simple lumped RC model of ESD protection devices using cadence (Virtuoso).
3. Worked with SPICE, process simulators (TSUPREM4, ISE-DIOS, 3-D TAURUS PROCESS), device simulators (MEDICI, ISE-DESSIS), Layout Editors (MAGIC and Cadence Virtuoso), Schematic Editors, Layout-vs.-Schematic tools.
4. Reviewer of research publications for in IEEE Transactions on Electron Devices, IEEE Transactions on Plasma Science, and IEEE Conferences, etc.

SEMINAR/CONFERENCES ATTENDED:

1. Attended and Presented our conference paper in VLSID-2016, Kolkata,
2. Attended and Presented our conference paper in CODEC-2015, Kolkata
3. Attended and Presented our conference paper in CCP-2015, Guwahati
4. Attended and Presented our conference paper in IWPSD-2015, Bangalore.

TECHNICAL SOCIETY MEMBERSHIP:

1. Member of IEEE Technical Society (From 01/01/2017 to Present)
2. Member of IEEE Electron Device Society (From 01/01/2017 to Present)
3. Student member of IEEE Technical Society (From 01/01/2013 to 31/12/2016)
4. Student Advisory Member of IEEE Student Branch, IIT GUWAHATI (From 01/01/2014 to 01/06/2017).

EXTRA CURRICULAR ACTIVITIES:

1. Organized workshop on "Introduction to MATLAB and its Applications" from 29/03/2019 and 30/03/2019 at IIIT Bhagalpur
2. Organized workshop on "Introduction to Robotics" from 08/03/2019 and 10/03/2019 at IIIT Bhagalpur
3. Organized Cultural program of IIIT Bhagalpur "SPANDAN-2K18"
4. Organized workshop on "Technical Training for Language Lab" from 13/10/2017 and 14/10/2017 at IIIT Bhagalpur.
5. Technical Volunteer in IEEE workshop in VLSI and MEMS Digital Design Flow 2014.
6. Technical Volunteer and Anchor in National Workshop GPU Programming and Application(GPA) organized by IIT Guwahati, IIT Bombay, CDAC Pune and NVIDIA.
7. Technical Volunteer in ADMAT-2015, 2016 organized by IIT Guwahati.
8. Student Volunteer in VDAT-2016 organized by IIT Guwahati.
9. Member of Event Manager in 49th Inter IIT Sports Meet – 2013.

PERSONAL DETAILS:

Name: Dheeraj Kumar Sinha
Father's Name: Avinash Kumar
Language: Hindi and English
D.O.B.: November10 1987
Passport Details: K1524690
PAN Card Details: CUXPS4268R

REFERENCES:

Dr. Gaurav Trivedi
Assistant Professor
Department of EEE,
IIT Guwahati
Email: **trivedi@iitg.ernet.in**

Prof. Ronald D. Schrimpf
Professor
Department of Electrical Engineering,
Vanderbilt University
Email: ron.schrimpf@vanderbilt.edu

Prof. Pinakeshwar Mahanta
Director & Professor
Department of Mechanical Engineering
NIT Arunachal Pradesh
Email: **pinak@iitg.ernet.in**

DECLARATION:

I hereby declare that all the information furnished above are true to the best of my knowledge and belief.

Date:

Dheeraj Kumar Sinha